ECE 35 Project 2 Digital to Analog Converter (DAC)

The objective of this project is to analyze, build, and test a 4-bit Digital to Analog Converter (DAC) based on an *R*/2*R* ladder network. DACs and their twin brother, ADCs are core components for any electronics with a microprocessor brain. Take digital cameras for example: The sensor behind the lens collects brightness and color information. These are analog signals that are subsequently converted to binary numbers via ADC for the processor to compute and record to the memory card. In the back of the camera, a DAC will read each digital input and restore them to corresponding analog levels to power each pixel on the LCD display with correct brightness and color. In this lab, an up-down counter will drive the DAC input and its output analog voltage will be measured with an oscilloscope. The up-down counter is a discrete CMOS chip which we will power with a 5V supply and clock with a square wave function generator. The counter will be tested with a logic analyzer.

A complete analog design project usually includes design, analysis, simulation, building, and testing. In this project a basic design is provided to you and we will skip the circuit simulation. Instead you will be performing analysis to confirm that the design is correct and then test the circuit.

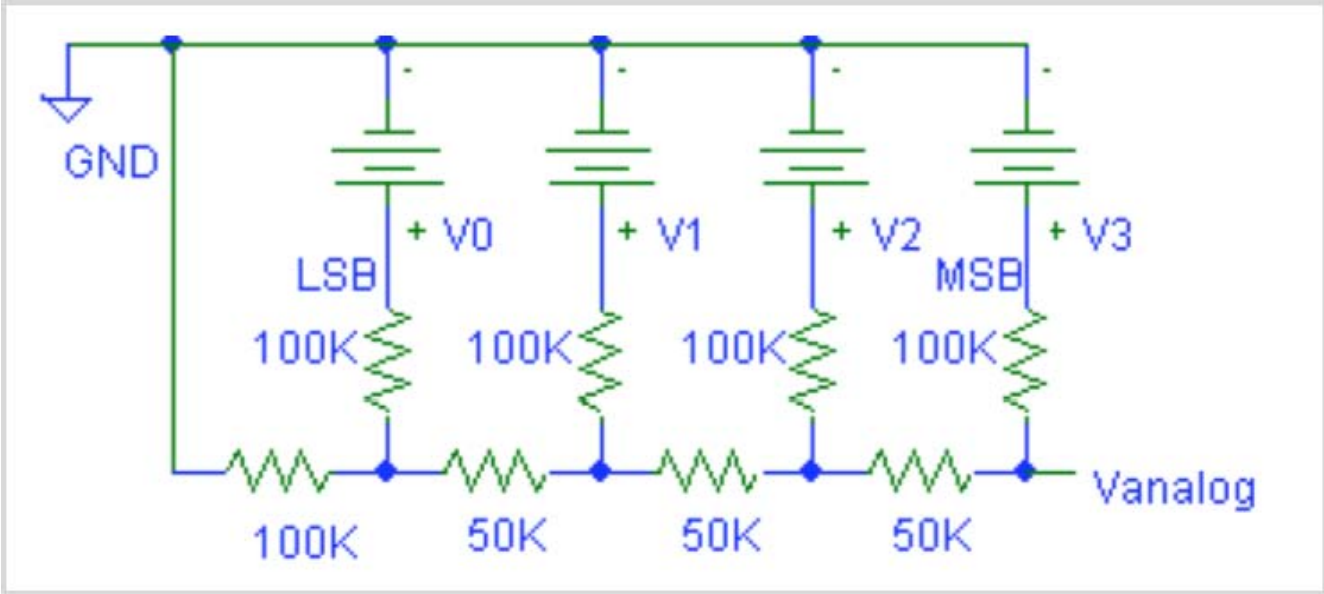
Prelab: You must complete the Analysis before the start of lab.

Report: As before you must write a report explaining exactly what you did in the lab and the results of your testing. This report must include hard copy plots demonstrating that the counter and the DAC work as expected. Your report should start with the analysis done in the prelab, and should answer any questions that are be directly asked in the instructions. The report should be written such that a technically literate person could repeat your work and obtain the same results.

Analysis: The *R*/2*R* ladder network shown below can be most easily (and therefore most accurately) analyzed using the **Superposition method**, since the circuit is linear. That is, you can calculate the output voltage, Vanalog, due to each source independently (with all the other voltage sources turned off), and sum the voltages from each source to obtain the final result. Here each voltage source (V0~V3) represents the voltage input from each digital output of the counter chip. They all supply the same voltage, but contribute to Vanalog differently based on their topology. Start with Vanalog $=\sum aV$. In calculating the output voltage of each source you should start with the most significant bit (MSB), solve the circuit for output (*V*analog) and then do the next most significant bit. You may then write an equation for the less significant bits using mathematical induction. You may also find that using using source transformation can be very helpful in simplifying the circuit solving steps. The final result will have the form:

$$\text{Vanalog} = a_0\text{V}_0 + a_1\text{V}_1 + a_2\text{V}_2 + a_3\text{V}_3.$$

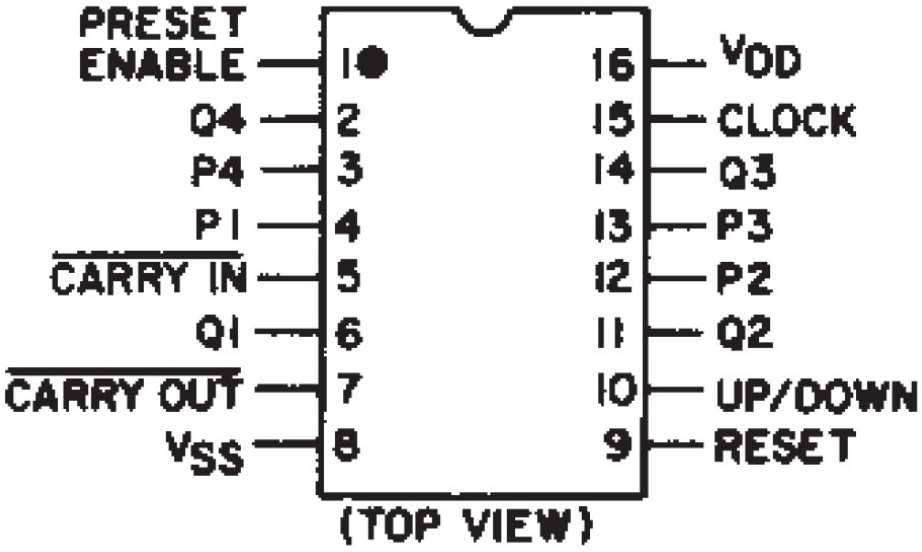
Explain in your report the method you chose to solve for Vanalog and discuss the result.



Counter: If you have not taken the equivalent of ECE25 you may not have seen a counter chip before. A counter is a sequential circuit that has *N* bits of memory, which can be considered an *N* bit binary word. When the CLOCK input rises from zero to one, the word is either incremented or decremented by one depending on the state of the UP/DOWN control. The counter we will use can also be loaded in parallel if PRESET_ENABLE is true. For this project you don't need to know how it is designed, but you need to know what it does. We will use the counter simply as a way of cycling through all-possible combinations of sources being off or on. More details on the counter 4516 chip can be found on the ECE25 website on ece-classweb. Go there and select the "datasheet and logic board" section from the left side navigation bar.

Logic Analyzer: The logic analyzer is an instrument you may not have seen before. You can think of it as a multi-channel O-scope for digital signals. It only measures whether the signal is on or off, whereas a scope measures the analog voltage. The strengths of a logic analyzer are that it can sample many more channels than the O-scope, and it can trigger on logical combinations of signals. For this project we will treat it simply as an 8-channel scope. Instead of scope probes you have a "pod" with 8 short signal wires and a ground. They can be connected to the circuit with mini-grabber hooks. Inputs you are not using can be left unconnected. The pod is connected to the USB port on a computer and the instrument controls are "virtual" panels on the computer. It is quite intuitive to operate, but you should plan to spend 5 minutes to familiarize yourself with it.

Testing: Turn the supply off while you are wiring the counter chip on the breadboard. Connect the function generator to the clock input (pin 15) and set it to provide a 0 to 5V square wave at a frequency of about 10 KHz. We will power Vdd (pin 16) and UP/DOWN (pin 10) with 5V from the power supply. Ground pins 1, 5, 8, and 9. The P1 – P4 (pins 3,4,12,and 13pins) can be left *not connected*. The MSB is Q4 and the LSB is Q1. These pins will connect to your R/2R ladder circuit and will serve as the sources. Keep the layout as clean as possible because it will simplify your debugging.



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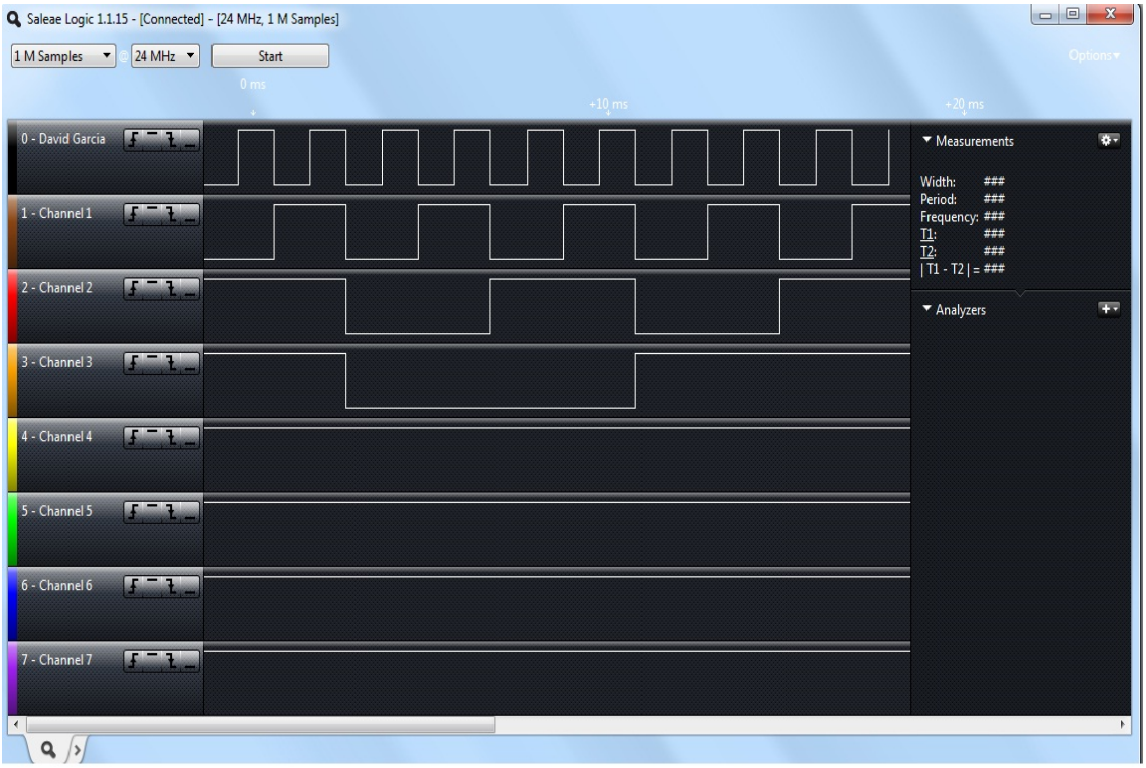
The *R*/2*R* ladder, where *R* = 50 kΩ, should be built using all 100 kΩ resistors. The 50 kΩ resistor can be made with two 100 kΩ resistors in parallel and will be more accurate than an independent 50 kΩ resistor. You will need a total of eleven 100 kΩ resistors. Once you have the circuit built, turn on your power supply and it set to 5V.

This part of the lab will get you in the habit of testing individual parts of your circuit. With the O-scope, measure the clock (pin 15), make sure you are able to read the frequency and pk-pk voltage on the display. Take note of those readings. Now take a measurement of the LSB output (Q1, pin 6) with the O-scope. The LSB should switch at half the frequency of the clock, and the pk-pk voltage should be relatively the same– if not there is an error and you need to find it before continuing. The most common error is that the supply voltage and ground pins on the CD4516 chip are not connected. Confirm that the voltage on these pins is correct with the DMM before continuing trouble-shooting. Confirm that the remaining outputs (Q2-Q4) have the same voltage and that the frequency is half the previous.

Now we'll use the logic analyzer to check the counter chip. We'll connect the clock and each of the four output bits to the logic analyzer and display the result on the computer screen. Hook the grey lead of the logic analyzer to ground, the black lead to the clock, the brown lead to the Q1, the red lead to the Q2, and the orange lead to Q3, the yellow lead to Q4. If a lead is missing or broken, it is OK to substitute another.

There is a program for the logic analyzer called "Logic". Find it through the start menu (All Programs ---> SALEAE LLC ---> Logic), or click on the desktop shortcut and open it. When it is opened it should look similar to the figure below, but will not have the same waveform.



Click the "Start" button. Use your mouse to zoom in and out (right click to zoom out and left click to zoom in). Adjust the logic analyzer sample interval until you can see a whole cycle of the MSB on the screen. Make a hard copy of the display. Change the up-down control to down by grounding pin 10 of the counter chip and confirm that it counts down correctly. Make another hard copy of the display. Have the TA sign you off for the hard copies.

You have checked that the counter is operating properly. Is it now time to check your circuit results. Remove the logic analyzer. Connect channel 1 of the O-scope to the MSB and channel 2 to your DAC Vanalog output. Press “Auto Set” and you should see Vanalog going through staircase shape repeatedly. If not, confirm that the resistors are grounded properly. When it is working correctly make a hard copy. Switch the up-down control and make another hard copy. Demonstrate your circuit to the TA and have your signature sheet signed off.

The DAC should work quite well with a clock frequency of 10 kHz, with Vanalog showing nice square steps. As you increase the clock frequency the edges of the step will become rounded and eventually, as you increase the clock frequency, Vanalog will be unable to track input changes and the DAC will become unusable. But the “roundness” of the steps is too arbituary. Find the frequency such that the bottom edge of Vanalog no longer reaches the zero volt line. Clearly our DAC is not usable at that point. Include this clock frequency in your report. Show your TA the result and have them sign your sheet

Discuss in your lab report:

- Discuss the relation between the symmetry of the ladder circuit and the equation you obtained for Vanalog. Would the expression of Vanalog change if the symmetry of the circuit were broken?
- Qualitatively explain the behavior of the counter chip, CD4516, and how it was utilized for this experiment.
- What are the advantages and disadvantages of using the logic analyzer instead of using an O-scope
- Qualitatively explain what changes you see when you change the voltage at pin 10 of the counter chip
- Explicitly explain why Vanalog has the "staircase" shape when you measured it with the O-scope
- Explain why increasing the frequency of the function generator altered the "staircase" shape of your output.